



CMR TECHNICAL CAMPUS

Kandlakoya (V), Medchal Road, Hyderabad-
501401



A Two Day Faculty Development Programme

On

Analog and Digital IC Design Using Mentor EDA Tool

3rd & 4th July 2018

Under Center for VLSI and Embedded System Design (CVESD)

Department of Electronics and Communication Engineering

Dr. P. Sireesha

Convener

Prof. G. Srikanth

HOD-ECE

Dr. A. Raji Reddy

Director

CMR TECHNICAL CAMPUS

(Accredited by NBA, Permanently Affiliated to JNTUH
& Approved by AICTE)
Kandlakoya (V), Medchal (M), Hyderabad - 501401



Two day Faculty Development program on “Analog & Digital IC Design using Mentor EDA Tools” 3rd & 4th July 2018 (Under CVESD Centre)



(3rd & 4th July, 2018)

**Organized By
Department of
ELECTRONICS & COMMUNICATION
ENGINEERING**

REGISTRATION FORM

Two day Faculty Development program on “Analog & Digital IC Design using Mentor EDA Tools 3rd & 4th July 2018

1. Name:
2. Teaching Experience:
3. A) Designation:
b) Department:
c) Institution:
d) Affiliating University:
4. Address for Communication:
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.....
5. Phones No's:
(O).....(R).....
E - Mail ID:

Chief Patron: Shri Ch. Gopal Reddy.
Chairman, CMRTC.

Smt. C. Vasantha Latha.
Secretary, CMRTC

Patron: Dr. A. Raji Reddy.
Director, CMRTC

Organizing Secretary: Prof. G.Srikanth.
HoD ECE

Convenor: Dr. P.Sireesha
Assoc.Professor, ECE

Faculty Coordinator: 1. Mrs.Sk.Dilshad
Asst. Professor, ECE
2.Ms. Karuna Sree
Associate Professor, ECE

CVESD Advisory board members:
Dr. Ashutosh Saxena .
Dean (R&D), professor,
CSE Department, CMRTC.

Organizing Committee:

Ms.V.Aswini Asst.Professor, ECE
Mr.T.Narendra kumar,Asst.Professor ECE
Mrs.B.Anita , Asst. Professor, ECE
Ms.Keerti Somraj, Asst .Professor, ECE
Mr.PA Irfan khan, Asst. Professor, ECE
Ms.N.Renuka Asst.Professor, ECE

RESOURCE PERSON:

Mr.Nagendra Bandi
Application Engineer
CoreEL Technologies Pvt,ltd
Bengaluru.

Date:

Signature

Name:

ABOUT THE COLLEGE

CMR Technical Campus has been structured to take a quantum leap on the changing trends of technology. The Campus is accredited by NBA in the year 2014. The need of setting up the college emerged when no other college could fulfil the aspirations of a student in his/her endeavour to acquire wholesome education. The very strength of CMR Technical Campus lies in its principles of providing the right learning environment for the student who does not have to compromise throughout the learning process of becoming global citizen. Over the years since it has been established, there has been dynamic progress at CMRTC in all academic and research activities, and a spectacular improvement in facilities and infrastructure, to keep it on par with the best institutions in India. The campus epitomizes the Technical Campus motto, "Learning and exploring" in providing the best of infrastructure and ambience. CMR Technical Campus keeps abreast of the global situation.

ABOUT THE DEPARTMENT

The Department of Electronics & Communication Engineering (ECE) established in year 2010 with an intake of 60 students, present intake of 180. Right from its inception it is continuously striving to impart quality education and promoting competitive spirit among the student for academic excellence. Department started M.Tech in Embedded Systems from Academic year 2012-13 with intake of 24.

Different centers of the department, periodically Organizing Seminar, Guest Lecture, Workshop by IIT Professor and Industry Expert, FDP and conferences.

ABOUT THE CENTRE:

Centre for VLSI & Embedded system design established in the year 2016 with an aim to build low cost, indigenous technologies through the research & development. Our object is to nurture the young engineers with all skills necessary for various aspects of computer systems development through research oriented projects.

It intensifies the practical skills of students and to be trained for present needs of VLSI and embedded industry. It renders right blend of class room teaching & bestowing the knowledge on ASIC & FPGA design flow using front end and back end tools.

ABOUT THE COMPANY

CoreEL Technologies is a technology company with businesses spread across design services & product development, distribution and training. Head Quartered in Bangalore, India, CoreEL is a leading provider of VLSI & Embedded System design services and Intellectual Property. Since its inception in 1999, CoreEL

Their Services offerings include Distribution of Silicon solutions, EDA tools, COTS products, Engineering Services (Turn Key Systems Design, Turn Key FPGA Design and High Speed PCB Design), Education and Manufacturing.

COURSE CONTENT

Implementation of Digital Circuits: Design of Basic gates, Combinational and Sequential Circuits using "EDL Tool".

Full Custom Design: Front End Verification & Physical Verification

Front End Verification: Simulation and Synthesis using EDA Tools

Physical Verification: Layout Design, Floor Planning, Routing, DRC, LVS.

Especially the following outcomes are derived from this two day course:

- Able to design the basic CMOS circuits and the process technology.
- This program also beneficial to faculty and who are looking for Research opportunities in the field of VLSI

Registration Fee: No registration fee

Important Dates:

FDP Date: 3rd&4th July 2018.

SPONSORSHIP CERTIFICATE

Certified that Dr./Mr. /Ms. _____ is an employee of our institution since _____. Presently he/she is working as _____, in the _____ department and is hereby sponsored for the one week FDP on "Analog & digital Ic design using mentor EDA tools." under the Centre for VLSI & Embedded System Design(CVESD)at Department of ECE, CMR Technical Campus,

Kandlakoya(V), Medchal Road, R. R. Dist. during the days 03-07-2018 and 04-07-2018.

Place:

**Signature of the
Principal/ Director
with Seal**

Date:

Contact:

Prof. G.Srikanth - 9248727226

Dr. P.Sireesha - 9959883215

Mrs. SK Dilshad – 9052009998

Ms. B Karuna Sree - 9160044360

**Email: hodececmrtes@gmail.com,
sirisha5716@gmail.com,
skdilshad.ece@gmail.com,
bkarunasree@gmail.com**

Website: www.cmrtc.ac.in



CVESD

(CENTER FOR VLSI AND EMBEDDED SYSTEM DESIGN)
DEPARTMENT OF ELECTRONICS &
COMMUNICATION ENGINEERING
CMR TECHNICAL CAMPUS

Kandlakoya (V), Medchal Road, Hyderabad-501401



CHIEF PATRON:

Sri. C. Gopal Reddy, Chairman

PATRONS:

Smt.C.Vasantha Latha, Secretary

Dr. Raji Reddy, Director

HOD

G.Srikanth, Professor, ECE Dept.

ADVISORY BOARD:

(1)**Dr.Ashutosh Saxena,**
Principal Research Scientist, Infosys
Limited,Hyderabad,
Dean(R&D),Professor, CSE Dept.,
CMR Technical Campus

(2)**Dr.Ahmed Ali Baig,**
Dean(Academics),Professor,
Mechanical Dept.,CMR Technical
Campus

Organizing Secretary:

Mr. Srikanth,
Professor, ECE HOD.

Convenor:

Dr. P sireesha,
Associate Professor

Faculty Coordinator:

1. Mrs.Sk.Dilshad

Asst. Professor, ECE

2. Ms.B. Karuna Sree

Assoc. Professor, ECE

Members:

Ms.V.Aswini

Asst.Professor, ECE

Mr.T.Narendra kumar

Asst.Professor ECE

Mrs.B.Anita ,

Asst. Professor, ECE

Ms.Keerti Somraj,

Asst .Professor, ECE

Mr.P. A. Irfan khan,

Asst. Professor, ECE

Ms.N.Renuka

Asst.Professor, ECE

Date : 02-07-18

To,

Kandlakoya, Hyderabad.

INVITATION

We the faculty members under CVESD from Electronics and Communication Engineering Department are organizing Two Day Faculty Development programme on "Analog & Digital IC Design using Mentor EDA Tools" scheduled from July 3rd to 4th July 2018 in association with ISTE Chapter. In this regard you are invited to attend the Inaugural function and grace the occasion with your kind presence at 10:00 am .

Venue: Room No: 331,'C' Block, ECE Department.

Program Inauguration By: **Mr.Nagendra Bandi**, Application Engineer,
CoreEL Technologies Pvt.Ltd, Bangalore.

About FDP:

The Proposed Faculty Development Programme (FDP) is based on **Implementation of Digital Circuits:** Design of Basic gates, Combinational and Sequential Circuits using "EDL Tool". **Full Custom Design:** Front End Verification & Physical Verification **Front End Verification:** Simulation and Synthesis using EDA Tools **Physical Verification:** Layout Design, Floor Planning, Routing, DRC, and LVS.

Prof.G.Srikanth

HOD,ECE

Dr. P Sireesha

CVESD Lead, Convener

Training schedule

On 3rd July 2018

Theory Session: (09 AM to 10 PM)

- Basics of ASIC Design and ASIC Vs FPGAs
- Full Custom Flow and Semi Custom Design Flow
- Latest Advancements VLSI Industry

Morning Session: (10:00 AM to 1:00 PM) Lab-1: Full Custom Design Flow

Schematic Entry, Spice Models, Simulation

DC Analysis and Measurement of Operation Point Analysis Transient and Power Analysis

Afternoon Session: (02: 00 PM to 4:30 PM) Lab-2: Layout entry

Floor planning, Placement, Routing

Physical Verification Using Industry Standard Calibre Tool (DRC, LVS, xRC) Summary and Queries

On 4th July 2018

Morning Session: (09:00 AM to 1:00 PM) Lab-3: Semi Custom Design Flow

Verilog Entry: Simulation and Synthesis, Layout Design From Verilog Netlist

Physical Design and Verification

Afternoon Session: (02: 00 PM to 4:30 PM) Lab-4: Cell Based Design

Designing XOR Gate with NAND Symbols

Layout of XOR cell by Preplaced Cells

Gallery



