CMR TECHNICAL CAMPUS

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CMR GROUP OF INSTITUTIONS

EXPLORE TO INVENT

VLSI Chip Design

Hands-on using Open Source EDA

Dates: 16th – 20th December, 2019

Course Contents:

RISC-V microprocessor based SoC using Magic layout tool, Standard Cell Library and design using SPICE, pre-layout timing analysis of SoC using open STA, Chip Planning using MAGIC, Hierarchial Placement/ Routing using pads and blocks using Magic.

Time: 09:30 AM – 04:00 PM

Venue: Room No.:331 (Computer Lab-2), C-Block

Organised by: CVESD, ECE Department

Global Coordinator:
Dr. Gaurav Trivedi
IIT Guahati

Local Coordinator
Dr. Mahesh V. Sonth
Ph. #: 9901669486

Resource Person:
Dr. H. S. Jatana
SCL-ISRO, Chandigarh

EVENT REPORT

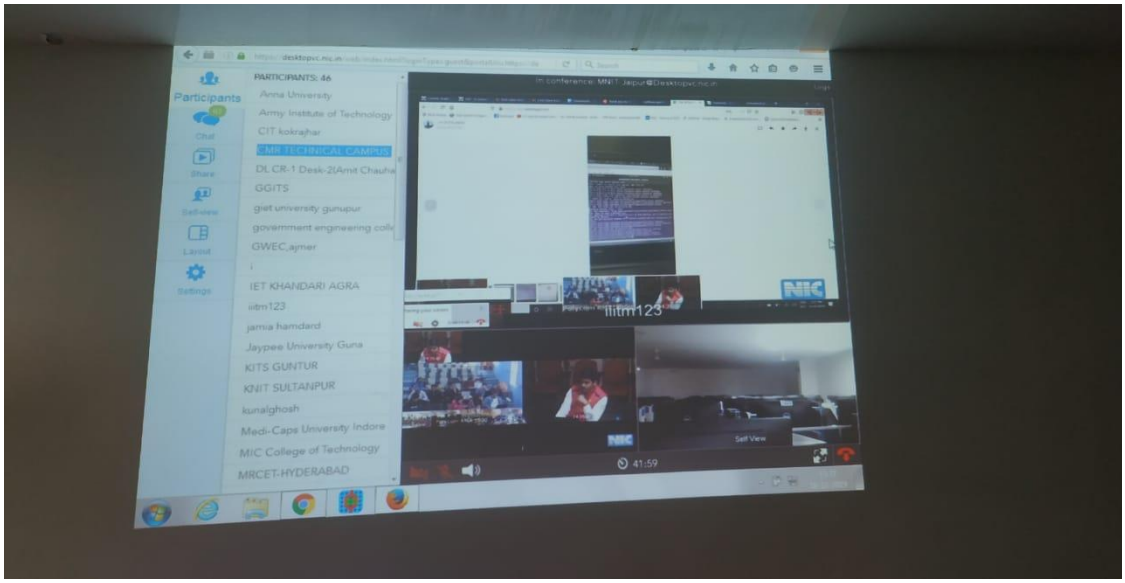
One Week faculty Development program on VLSI chip desgn –hands on usig open source
(16th – 20th December 2019)

Date: 22/12/2019

Participants from Various institutes of Telangana, attended in one week faculty development program on VLSI chip design –hands on using open source EDA . This program was conducted by IIT GUWAHATI as a HOST institute in association with Ministry of electronics and Information technology whereas CMR technical campus as Remote centre. In this program Prof.Vineet Sahula has enlightened the concepts called study of various components of Risc- V microprocessor in first day , and continued with standard cell library design &characterize one cell using Magic lay out control and ngSPICE simulations in the following day.

Third day (18/12/2019) session continued with pre lay out timing analysis of SoC using open STA chip planning with magic and block level placement .Fourth day(19/12/2019) with hierarchical placement/routing using pads and blocks, sign off checks,LVS/DRC checks. Fifth day(20/12/2019) session was about post-layout timing analysis using open STA and ECO using Tritansizer.Certificates received from the host institue and session completed.

Conveners


PARTICIPANTS: 46
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Anna University
Army Institute of Technology
CIT kokrajhar
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