SET-II

Subject Code: 19CS301ES

HT NO:

7 R

CMR TECHNICAL CAMPUS

UGC AUTONOMOUS

B. Tech. III Semester Supply End Examinations, July/August-2023 Analog and Digital Electronics Common to CSE&IT

Time: 3 Hours

Note

- i. This Question paper contains Part- A and Part- B.
- ii. All the Questions in Part A are to be answered compulsorily.
- iii. All Questions from Part B are to be answered with internal choice among them.

PART-A

 $10 \times 02 = 20 \text{ Marks}$

Max. Marks: 70

		•	Marks	CO	BL
1.	a	Write diode switching times? Write Difference between Half wave & Full wave Rectifier	2 M	CO1	L1
	b	whie Difference between Hall wave & Full wave Recurrer	2 M	CO1	L2
	С	Which is the most commonly used transistor configuration? Why?	2 M	CO2	L1
	d	Write the condition for thermal runaway	2 M	CO2	L3
	е	What are the differences between JFET & BJT	2 M	CO3	L2
	f	Define drain resistance	2 M	CO3	L1
	g	Define logic gates?	2 M	CO4	L·1
	h	State De Morgan's theorem.	2 M	CO4	L3
	i	What are the classifications of sequential circuits?	2 M	CO5	L2
	j	Give the comparison between combinational circuits and sequential circuits.	2 M	CO5	L1

PART-B

 $5 \times 10 = 50 \text{ Marks}$

			Marks	CO	BL
2.	a	Explain forward bias and reverse bias in a PN junction and also VI characteristics of PN junction.	6 M	CO1	L2
	Ъ	Explain the operation of photo diode with neat diagram OR	4 M	CO1	L1
3	a b	Explain the operation of Half wave Rectifier with neat wave forms Discuss the effect of temperature on PN junction Diode	6 M 4 M	CO1 CO1	L1 L3
4	a b	Explain the current components of a transistor Explain how transistor acts as an amplifier	6 M 4 M	CO2 CO2	L1 L2

OR

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5	a b	Compare CE, CB & CC Co With neat sketch explain Re	•		5 M 5 M	CO2 CO2	L4 L2
6	6 a With neat diagram explain the operation of TTL gates OR			10 M	CO3	L4	
. 7	a b	What are the applications of Explain briefly RTL and DO	f JFET?		6 M ·4 M	CO3 CO3	L3 L2
8	a	Simplify the following f(A,B,C,D,E)= Σ (3,6,7,8)	_		10 M	CO4	L5
9			10 M	CO4	L5		
10	0 a	Construct a JK flip flop using a D flip flop and other logic gates With the help of Truth Table/Timing Diagram, explain 3-bit Ripple counter using JK flip-flop		5 M 5 M	CO5 CO5	L6 L6	
11	1 a	OR With the help of neat diagram, explain different Shift Registers		10 M	CO5	L3	
C	0	: Course Outcomes					
В	L	: Bloom's Taxonomy Levels	L1: Remembering	L 2 : Underst	anding		
			L 3 : Applying	L 4 : Analysir	ng		
			L 5 : Evaluating	L 6 : Creating	5		
