

## CMR TECHNICAL CAMPUS

## UGC AUTONOMOUS

B. Tech. III Semester Supply End Examinations, July/August-2023

Computer Organization and Architecture

Department of CSE

Time: 3 Hours

Max. Marks: 70

## Note

- i. This Question paper contains Part- A and Part- B.
- ii. All the Questions in Part A are to be answered compulsorily.
- iii. All Questions from Part B are to be answered with internal choice among them.

\*\*\*\*\*

## PART-A

10 X 02 = 20 Marks

		Marks	CO	BL
1.	a	2	CO1	L2
	b	2	CO1	L1
	c	2	CO2	L1
	d	2	CO2	L1
	e	2	CO3	L2
	f	2	CO3	L4
	g	2	CO4	L1
	h	2	CO4	L3
	i	2	CO5	L3
	j	2	CO5	L4

## PART- B

5 X 10 = 50 Marks

		Marks	CO	BL
2.	a	5	CO1	L3
	b	5	CO1	L3
	OR			
3	a	5	CO1	L2
	b	5	CO1	L2
4	a	5	CO2	L2
	b	5	CO2	L2

OR

(17)

- |    |   |  |   |     |    |
|----|---|--|---|-----|----|
| 5  | a | Explain about the address sequencing in control memory with neat diagrams?   | 5 | CO2 | L2 |
|    | b | Explain about data transfer and manipulation.  | 5 | CO2 | L2 |
| 6  | a | Draw flow chart for multiplication of two floating point numbers.  | 5 | CO3 | L2 |
|    | b | Explain various Decimal arithmetic operations.   | 5 | CO3 | L2 |
| OR |   |  |   |     |    |
| 7  | a | Explain how complement number system is useful in computer system. Discuss any one complement number system with example | 5 | CO3 | L3 |
|    | b | Explain about the multiplication algorithms in Computer Arithmetic.  | 5 | CO3 | L2 |
| 8  | a | Explain DMA Controller with the block diagram?   | 5 | CO4 | L2 |
|    | b | Define Random Access Memory and explain various types of RAMs present?   | 5 | CO4 | L2 |
| OR |   |  |   |     |    |
| 9  | a | Explain the mapping procedures adopted in the organization of a Cache Memory?  | 5 | CO4 | L2 |
|    | b | Discuss memory mapped I/O in computer organization?  | 5 | CO4 | L2 |
| 10 | a | Explain three segment instruction pipelines with the help of timing diagram.   | 5 | CO5 | L3 |
|    | b | Describe system bus structure for multiprocessors.   | 5 | CO5 | L2 |
| OR |   |  |   |     |    |
| 11 | a | Explain pipeline for floating point addition and subtraction.  | 5 | CO5 | L2 |
|    | b | Describe cache coherence and why is it important in shared memory multiprocessor systems?                                | 5 | CO5 | L4 |

CO : Course Outcomes

BL : Bloom's Taxonomy Levels

L 1 : Remembering

L 2 : Understanding

L 3 : Applying

L 4 : Analysing

L 5 : Evaluating

L 6 : Creating

\*\*\*\*\*