

## CMR TECHNICAL CAMPUS

## UGC AUTONOMOUS

B. Tech. III Sem Regular End Examinations, February-2024 ✓

Computer Organization &amp; Architecture ✓

Common to CSE, IT, CSC, CSM, CSD &amp; AIML ✓

Time: 3 Hours

Max. Marks: 60 ✓

## Note

- i. This Question paper contains Part- A and Part- B.
- ii. All the Questions in Part A are to be answered compulsorily.
- iii. All Questions from Part B are to be answered with internal choice among them.

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## PART-A

10 X 01 = 10 Marks ✓

		Marks	CO
1.	a	1M	CO1
	b	1M	CO1
	c	1M	CO2
	d	1M	CO2
	e	1M	CO3
	f	1M	CO3
	g	1M	CO4
	h	1M	CO4
	i	1M	CO5
	j	1M	CO5

## PART- B

5 X 10 = 50 Marks

		Marks	CO
2.	a	5M	CO1
	b	5M	CO1
	OR		
3.	a	5M	CO1

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|----|---|---|----|-----|----|
|    | b | Describe the process of register transfer and its relationship to data movement within a computer system. and processing in a digital computer system.                            | 5M | CO1 | L2 |
| 4  | a | Explain the importance of various types of instructions and addressing modes in designing an effective ISA?   | 5M | CO2 | L2 |
|    | b | Define microprogrammed control and explain its advantages and limitations compared to hardwired control.  | 5M | CO2 | L2 |
| OR |   |   |    |     |    |
| 5  | a | Describe the purpose and functions of computer registers in a digital computer system.  | 5M | CO2 | L2 |
|    | b | explain the significance of address sequencing in the context of a microprogrammed control unit?  | 5M | CO2 | L2 |
| 6  | a | Discuss the significance of rounding modes in floating-point arithmetic operations and explain how do rounding modes affect the accuracy and precision of numerical computations? | 5M | CO3 | L3 |
|    | b | Explain the concept of relative addressing and its importance in supporting position-independent code.  | 5M | CO3 | L2 |
| OR |   |   |    |     |    |
| 7  | a | Explain the role of general-purpose registers in a CPU.   | 5M | CO3 | L2 |
|    | b | Describe the process of division in computer arithmetic, including algorithms like restoring division and non-restoring division.   | 5M | CO3 | L3 |
| 8  | a | Define cache memory and explain its role in improving system performance.   | 5M | CO4 | L2 |
|    | b | Compare and contrast synchronous and asynchronous data transfer methods.  | 5M | CO4 | L2 |
| OR |   |   |    |     |    |
| 9  | a | Discuss the importance of associativity in cache memory and how it affects cache performance.   | 5M | CO4 | L2 |
|    | b | Define priority interrupt and its significance in I/O operations.   | 5M | CO4 | L2 |
| 10 | a | Describe how RISC architectures achieve efficiency and performance improvements compared to CISC architectures.   | 5M | CO5 | L2 |
|    | b | Define vector processing and its advantages in handling array-based computations.   | 5M | CO5 | L2 |
| OR |   |   |    |     |    |
| 11 | a | List the key characteristics of RISC architectures.   | 5M | CO5 | L2 |
|    | b | Describe the concept of instruction pipelining and its impact on instruction throughput.  | 5M | CO5 | L2 |

**CO : Course Outcomes**

**BL : Bloom's Taxonomy Levels**

<b>L 1 : Remembering</b>	<b>L 2 : Understanding</b>
<b>L 3 : Applying</b>	<b>L 4 : Analysing</b>
<b>L 5 : Evaluating</b>	<b>L 6 : Creating</b>

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