CMR TECHNICAL CAMPUS
UGC AUTONOMOUS
B.Tech - IV Semester, Regular End Examinations, July-2022
Analog and Digital Electronics (20EC402PC)
(Common to CSM & CSD)

Time: 3 Hours   Max. Marks: 70

Answer Any Five Questions
All Questions Carry Equal Marks .

5 X 14 = 70 Marks

1. a. With the help of a neat circuit diagram, explain the working of an series biased clipper. [7M]
   b. Explain the characteristics, working & Volt Ampere Characteristics of Tunnel diodes, [7M]

2. a. Explain the construction, working and characteristics of Photo Diode? [7M]

   b. State and prove the clamping circuit theorem? [7M]

3. a. Explain the operation of FET with its characteristics and explain the different regions in transfer characteristics? [7M]

   b. Define pinch-off voltage and trans conductance in field effect transistors? [7M]

4. a. Explain how a FET can be made to act as a voltage variable resister? [7M]

   b. Bring out the differences between FET and MOSFET. Draw the circuit diagram of CS JFET amplifier? [7M]

5. a. Explain the working of CMOS as an inverter? [7M]
   b. Draw the basic TTL logic NAND gate and explain it. [7M]

6. a. Design a two-input NOR and two-input NAND using DTL logic. [7M]

   b. Compare different logic families [7M]

7. a. Summarize the Boolean function $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15) + d(w, x, y, z) = \Sigma(0, 2, 5)$ [7M]

   b. Use a multiplexer having three data select inputs to solve the logic for the function $F = \Sigma(0, 1, 2, 3, 4, 10, 11, 14, 15)$ [7M]

8. a. Explain the state reduction, state assignment with an example. [7M]
   b. Design a 4-bit BCD Ripple Counter by using T-FF? [7M]

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CMR TECHNICAL CAMPUS
UGC AUTONOMOUS
B. Tech. IV Semester Supply End Examinations, February-2024
Analog and Digital Electronics
Common to CSM, CSD, AIML, CSG

Time: 3 Hours   Max. Marks: 70

Note
   i. This Question paper contains Part- A and Part- B.
  ii. All the Questions in Part A are to be answered compulsorily.
 iii. All Questions from Part B are to be answered with internal choice among them.

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PART-A

10 X 02 = 20 Marks

			Marks	CO	BL
1.	a	Describe the different types of clipper circuit.	2	CO1	L1
	b	What is the principle of operation of photodiode?	2	CO1	L1
	c	Write the comparison between BJT and FET?	2	CO2	L1
	d	Draw the drain characteristics of depletion type MOSFET?	2	CO2	L1
	e	Implement OR gate using NAND gates only.	2	CO3	L3
	f	Draw CMOS NAND gate	2	CO3	L1
	g	Which gates are universal gates and why they are called?	2	CO4	L1
	h	Write a short notes on priority encoder	2	CO4	L1
	i	Differentiate between Latch and flip flop.	2	CO5	L2
	j	What are the basic types of shift registers?	2	CO5	L1

PART- B

5 X 10 = 50 Marks

			Marks	CO	BL
2.		From the Energy band diagram explain the V-I characteristics of a tunnel Diode. List the applications of tunnel diode.	10	CO1	L2
		OR			
3	a	With the help of a neat circuit diagram, explain the working of a two-level diode clipper	5	CO1	L2
	b	Discuss the effect of diode characteristics on clamping circuits	5	CO1	L2
4	a	With the help of neat sketches and characteristic curves explain the construction & operation of JFET and mark the regions of operation on the characteristics?	5	CO2	L2
	b	Compare the three configurations of JFET amplifiers?	5	CO2	L2

OR

5	a	Discuss the theoretical operation CS FET amplifier.	5	CO2	L1
	b	Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?	5	CO2	L2
6	a	Perform The Following Conversions i)$(AB)_{16}$=( )$_{10}$ ii)$(123)_8$=( )$_{10}$ iii)$(346)_8$= ( )$_2$ iv)$(100011001)_2$=( )$_{16}$	5	CO3	L3
	b	Show that the dual of the Exclusive – OR is equal to its complement.	5	CO3	L2

OR

7	a	Describe the operation of DTL NAND Gate	5	CO3	L2
	b	Realize 2-input OR gates using CMOS logic and then explain its operation with the help of functional table.	5	CO3	L2
8	a	Minimize the following expression using K-map and realize using NAND Gates. F (A,B,C,D) = $\sum m (0,1,2,9,11)$ +d(8,10,14,15).	5	CO4	L2
	b	Simplify the following Boolean expressions to a minimum number of literals (i) ABC+A'B+ABC' (ii) xy + x(wz+wz')	5	CO4	L3

OR

9	a	Design and explain a 4-bit binary parallel Adder/Subtractor.	5	CO4	L3
	b	Define a multiplexer? Draw a 2:1 multiplexer for the function $f(x,y,z)$=$\sum(0,2,3,5,7)$	5	CO4	L3
10	a	Explain the operation SR flip flop. Explain its truth table.	5	CO5	L2
	b	Find the characteristic equation for: i) T flip-flop ii) D flip-flop	5	CO5	L1

OR

| 11 | a | Design Mod-10 Synchronous counter using T flip-flop. | 5 | CO5 | L3 |
| | b | Design a 3 bit Ripple counter. | 5 | CO5 | L3 |

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