CMR Technical Campus

B.Tech Mid Question Bank (R22 Regulation)

Academic Year: Semester:2024-2025

Subject Name: Computer Organization and Architecture

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PART-A

MID-I Questions					
Q.No	**Questions**	**Marks**	**BL**	**CO**	**Unit No**
1	Draw the block diagram of a Register.	2	L1	CO1	I
2	Draw a block diagram of computer	2	L1	CO1	I
3	Convert the AB.CD to binary, octal, decimal.	2	L2	CO1	I
4	Define Register transfer with example.	2	L1	CO1	I
5	Obtain the l's and 2's complements of the following eight-digit binary numbers: 10101110; 10000001; 10000000; 00000001.	2	L2	CO1	I
6	Define Program Counter and Accumulator.	2	L2	CO1	I
7	Define Instruction code and Instruction format.	2	L1	CO2	II
8	Write the differences between hardwired control and micro programmed control unit.	2	L1	CO2	II
9	Explain Instruction set Completeness.	2	L2	CO2	II
10	Write three types of Instruction formats.	2	L1	CO2	II
11	Write a short note on stored program organization.	2	L1	CO2	II
12	Explain the importance of control memory.	2	L2	CO2	II
13	Write Zero address Instructions for the expression A*B+C.	2	L1	CO3	III
14	What are the differences between addressing modes and instruction formats?	2	L1	CO3	III
15	What is Indexed Addressing Mode?	2	L1	CO3	III
MID-II Questions					
16	Draw the Hardware for sign Magnitude Addition and Subtraction.	2	L1	CO3	III
17	What is overflow in computer arithmetic?	2	L1	CO3	III
18	List all possibilities of addition and subtractions of two number.	2	L1	CO3	III
19	What is write back, write through, in cache?	2	L1	CO4	IV

20	What do the major differences exist in for the communication between central computer and peripheral?	2	L1	CO4	IV
21	Draw the RAM and ROM block diagrams.	2	L1	CO4	IV
22	What is Cycle stealing in DMA?	2	L1	CO4	IV
23	What is auxiliary memory? Give two examples.	2	L1	CO4	IV
24	What is interrupt?	2	L1	CO4	IV
25	Write one solution for cache coherence problem.	2	L1	CO5	V
26	What are the characteristics for multi-processors?	2	L1	CO5	V
27	Write two solutions to handle data dependency in pipeline Hazards?	2	L1	CO5	V
28	How do we establish communication link from one processor to another processor in Hyper cube inter connection?	2	L1	CO5	V
29	What is pipeline ?	2	L1	CO5	V
30	Draw the instruction pipeline grant chart without any hazards	2	L1	CO5	V

PART-B

MID-I Questions					
Q.No	**Questions**	**Marks**	**BL**	**CO**	**Unit No**
1	Explain about Computer Architecture, Computer Organization, Computer Design.	4	L2	CO1	I
2	Explain about Logic Micro Operations.	4	L1	CO1	I
3	Explain about Arithmetic Logic Shift Unit.	4	L5	CO1	I
4	What is micro-operation. Write different types of it.	4	L1	CO1	I
5	What are the differences between fixed point representation and floating-point representation	4	L2	CO1	I
6	Draw and explain Arithmetic circuit	4	L1	CO1	I
7	Conversion of Decimal into Binary i) 595.6875 ii) 8795, Decimal into Hexadecimal i)1595 ii) 8795,Decimal into octal i)142 ii) 763	8	L3	CO1	I
8	Explain about Bus and memory transfer.	8	L1	CO1	I
9	Explain about 16 Logic Micro operations?	8	L6	CO1	I
10	Draw Control unit of a basic computer	4	L1	CO2	II
11	What are the different types of Computer Registers and write their function.	4	L1	CO2	II
12	Explain about Instruction code.	4	L2	CO2	II
13	Explain about Micro Program example.	4	L2	CO2	II
14	Discus about Instruction Cycle.	4	L6	CO2	II
15	Explain and Input Output instructions.	4	L1	CO2	II
16	Discus different types memory reference instructions	8	L6	CO2	II
17	Explain program interrupt and interrupt cycle.	8	L1	CO2	II

18	Discuss about timing and control unit.	8	L2	CO2	II
19	Explain Instruction formats.	4	L2	CO3	III
20	Explain Control Word.	4	L2	CO3	III
21	Explain any 4 addressing modes.	4	L2	CO3	III
22	Explain general register organization with example.	4	L2	CO3	III
	MID-II Questions				
23	Draw Hardware Implementation for Booth's Multiplication Algorithm and also Evaluate Booth's Multiplication for the following Multiplicand BR=10111, Multiplier QR=10011?	4	L2	CO3	III
24	Explain overflow and underflow in computer arithmetic using Examples.	4	L2	CO3	III
25	Explain the Addition and Subtraction algorithm along with its hardware implementation.	4	L1	CO3	III
26	Draw the flow chart of Booths algorithm.	4	L2	CO3	III
27	Explain Cache direct mapping technique.	4	L2	CO4	IV
28	Explain Cache memory set associative mapping.	4	L2	CO4	IV
29	Explain Cache Initialization.	4	L2	CO4	IV
30	Describe Memory Hierarchy.	4	L6	CO4	IV
31	Explain Asynchronous data transfer.	4	L2	CO4	IV
32	What Priority Interrupt. Explain it with neat diagram.	4	L1	CO4	IV
33	What is Content Addressable Memory. Explain its working with neat diagram.	8	L1	CO4	IV
34	Explain the development idea of Cache Memory.	8	L2	CO4	IV
35	What is DMA ?,Describe about it with neat diagram and compare Strobe control method and Handshaking method in Asynchronous Data Transfer.	8	L1	CO4	IV
36	Write short notes on Vector Processing.	4	L1	CO5	V
37	What is parallel processing. Explain Arithmetic pipeline.	4	L1	CO5	V
38	Explain the interconnection structure Multistage Network.	4	L2	CO5	V
39	Explain Cache Coherence problem with an example.	4	L2	CO5	V
40	Write the differences between RISC & CISC.	4	L2	CO5	V

41	Explain Hypercube interconnection structure	4	L2	CO5	V
42	Explain different types cache memory mappings	8	L2	CO5	V
43	Define and List out Interconnection Structures in Multiprocessor System and Elaborate Timeshared Common bus and crossbar switch	8	L2	CO5	V
44	Explain about the Pipeline organization for floating point addition and subtraction.	8	L1	CO5	V