Department of ECE

B. Tech. Mid Question Bank (R22 Regulation)

Academic Year: 2024-2025 **Semester: III**

Subject Name: Digital System Design [22EC302PC]

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PART A

MID-I Questions				
QN	Questions	Marks	BL	CO
1	Write the numbers 7, 5 and 4 in terms of following weighted binary codes a) 4,2,2,1 b) 8,4,2,1 c) 2,4,2,1	2M	L2	CO1
2	Find the value of base r if a) $(121)_r=(144)_8$ b) $(159)_{10}=(186)_r$	2M	L2	CO1
3	Why NAND/NOR gates are called universal gates? Derive all basic gates using universal gates.	2M	L1	CO1
4	Convert the given binary number to equivalent Gray code 0011 0101 1110 0010.	2M	L2	CO1
5	Convert $(8E47.AB)_{16}$ to binary, octal.	2M	L1	CO1
6	Perform the subtraction (42) - (68) using signed 2's complement representation.	2M	L1	CO1
7	Explain Half adder and Full Adder with truth table.	2M	L1	CO2
8	What is Multiplexer and Demultiplexers explain.	2M	L2	CO2
9	Explain 8 to 3 priority encoders.	2M	L4	CO2
10	Explain Half Subtractor and Subtractor with truth table.	2M	L1	CO2
11	What is Decoder? Write a truth table of 2 to 4 decoder.	2M	L2	CO2
12	Realize full adder function using K-map.	2M	L1	CO2
13	Difference between combinational and Sequential circuit.	2M	L1	CO3
14	Difference between latch and Flip-flop.	2M	L2	CO3
15	Difference between synchronous and asynchronous counter.	2M	L4	CO3
MID-II Questions				
16	What are the different types of shift registers and Mention applications.	2M	L1	CO3
17	Design Ring and Twisted Ring counter.	2M	L2	CO3
18	Write excitation table of JK flip-flop.	2M	L1	CO3
19	Differentiate Mealy and Moore model.	2M	L1	CO4
20	What do you mean by Parity?	2M	L2	CO4
21	List out the FSM capabilities and Limitations.	2M	L4	CO4
22	Explain Moore model with example.	2M	L1	CO4
23	Explain Mealy model with example.	2M	L2	CO4
24	What do you mean by Mod-N counters.	2M	L1	CO4
25	Design CMOS transmission gate.	2M	L1	CO5
26	Compare various logic families.	2M	L2	CO5
27	Design NAND gate using diodes and transistors.	2M	L4	CO5
28	Design TTL open collector output circuit.	2M	L1	CO5
29	What is Tristate Logic in TTL?	2M	L2	CO5
30	Design TTL NAND gate.	2M	L1	CO5

PART- B

MID-I Questions				
QN	Questions	Marks	BL	CO
1	Encode the message bits (1011)2 into 7-bit even parity hamming code.	4M	L2	CO1
2	Convert the following expression into sum of products and product of sums. X'+X(X+Y') (Y+Z').	4M	L1	CO1
3	Implement EX-NOR gate using NAND logic.	4M	L2	CO1
4	Implement the following function using AOI logic F=BC'+AB+ACD	4M	L2	CO1
5	Simplify the following Boolean expressions using the Boolean theorems to minimum number of literals i) (BC'+A'D)(AB'+CD') (ii) (A'+C) (A'+C') (A+B+C'D)	4M	L2	CO1
6	Prove that Xs-3 code is a self-complementing code.	4M	L3	CO1
7	Obtain dual of the following Boolean expressions i) AB+A(B+C) +B'(B+D) ii) A+B+A'B'C. Obtain the compliment of the following Boolean expressions i) A'B+A'BC'+A'BCD+A'BC'D'E ii) ABEF+ABE'F'+A'B'EF.	8M	L2	CO1
8	i)State and Prove DeMorgans Theorem. ii)The Hamming code 101101101 is received. Correct if any errors. There are four parity bits and odd parity is used.	8M	L2	CO1
9	i)Expand A+BC'+ABD'+ABCD to minterms and maxterms. ii)Realize the Boolean expression using NAND only F=(AB+A'B') (CD'+C'D).	8M	L3	CO1
10	Minimize the following functions using k map F(A,B,C,D) = ∑ m(0,1,2,5,8,15) + d(6,7,10) F (A,B,C,D) = ∏ M(0,1,3,56,7,9,10,11,12,13,15)	4M	L2	CO2
11	Write down the simplified Boolean Expression in SOP and POS for F(A,B,C,D) = ∑ m(1,4,6,9,10,11,14,15) F(A,B,C,D) = ∑ m(,1,3,5,6,7,9,10,11,12,13,15)	4M	L1	CO2
12	Minimize the expression f = ∑ m(0,2,3,4,5,6) using k map and implement AOI logic as Well as NAND logic.	4M	L2	CO2
13	Minimize the following expressions using K-map and realize using NAND Gates. f = Σ m (1, 3, 5, 8, 9, 11, 15) +d (2, 13).	4M	L2	CO2
14	Minimize the following expressions using K-map and realize using NOR Gates. f = Σ m (1, 3, 5, 8, 9, 11, 15) +d (2, 13).	4M	L2	CO2
15	For the given function, obtain minimal SOP expression using K Map F (A, B, C, D, E) = ∑ m (6,9,13,18,19,25,27,29,31) + d∑ m (2,3,11,15,17,24,28). and implement it using NAND logic	4M	L3	CO2
16	Design a combinational circuit that converts 4-bit binary number into Grey code Converter.	8M	L3	CO2
17	Implement Full adder and 4 bit parallel Subtractor.	8M	L2	CO2
18	Design 2-bit Magnitude Comparator and Encoder for Octal to Binary.	8M	L3	CO2

19	Convert JK to D flip-flop.	4M	L1	CO3
20	Write excitation table of SR flip-flop.	4M	L2	CO3
21	Explain Master-Slave JK flip-flop.	4M	L3	CO3
MID-II Questions				
22	Design Mod 10 asynchronous counter using T Flip Flop.	4M	L2	CO3
23	Design 3-bit synchronous UP counter.	4M	L3	CO3
24	Explain the working of Bidirectional Shift Registers with the help of Diagram.	4M	L2	CO3
25	What is state diagram and state table explain with the help of example.	4M	L2	CO4
26	Explain state Reduction with the help of example.	4M	L2	CO4
27	Draw State Diagrams for D and T Flip Flops.	4M	L1	CO4
28	Design and Explain Serial Binary adder using Mealy model.	4M	L2	CO4
29	Design Sequence detector circuit using Mealy model.	4M	L1	CO4
30	Explain Mod-6 Synchronous counter.	4M	L2	CO4
31	Explain Mealy and Moore Models with Examples.	8M	L2	CO4
32	Design 3bit overlapped odd parity detector circuit using Mealy Model.	8M	L2	CO4
33	Design synchronous BCD (Mod-10) counter.	8M	L3	CO4
34	Realize basic logic gates using Diodes.	4M	L2	CO5
35	Design DTL NAND gate and explain working.	4M	L2	CO5
36	Design CMOS NAND and NOR gates	4M	L1	CO5
37	Design RTL NAND gate and explain working.	4M	L1	CO5
38	Realize basic logic gates using Transistors.	4M	L2	CO5
39	Explain Classification of IC.	4M	L2	CO5
40	Design TTL NAND gate circuit and Explain working of the same.	8M	L2	CO5
41	Design NOR gate using CML Logic Family.	8M	L2	CO5
42	Give a brief comparison between various logic families and define all parameters.	8M	L3	CO5